ASIC Hardware Implementation of Dual Mode Traffic Light Control

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ABSTRACT

This present work describes an ASIC Hardware Implementation of Dual Mode traffic light control. With this device, the logic operation is controlled or operated by two modes. In Mode-1, the system is operated with perfect period of timing and proper sequence states rotation automatically. In Mode-2, system operated desired states or roads directly. The device is designed in CMOS logic transistors and also logic gates. We developed the 90nm technology Layout. This simple optimized, low voltage and cost effective ASIC device finds potential application in every four-road junctions as well as to teach traffic lights observation demo classes.

KEYWORDS: ASIC, 90nm, CMOS, Layout and Dual Mode.

1. INTRODUCTION

Many works had done on the safety-optimized devises for traffic control at different kind of road junctions for better control signaling states. The main purpose of this traffic light control is to under stand even illiterate persons how to cross the road junctions according to the signals safely and without traffic-jams [1]. Therefore, to improve the traffic controlling, we have needed a new technique and logic system.

In the present work, a system was designed in this contest, which can operate with automatic clock generator circuit and with pressing switch circuit (a person needed to operate it). This new device given name is “Dual Mode”, which can apply easily at the road junctions. In this ASIC device, first select the mode of operation by controlling the Mode-Mux, then the main clock-in pulses will be divided in to seconds, minutes and road states by using Mod-Counters, these signals are fed to the Mid-Decoder which will gives the final outputs to control the traffic lights with proper timing and perfect state sequence rotation. In the other hand by feeding the Mid-Encode-Switch control signals to the Mid-Decoder, the junction states can operate by pressing the desired state switch directly, i.e. the operator decides timing of each state. ASIC system contains a Loudspeaker, which gives the sound before changing the signal from present state to the next state. In this way this newly developed ASIC device can improve the traffic light operation performance [2]. Figure-1 shows the road junction view to apply this ASIC device.

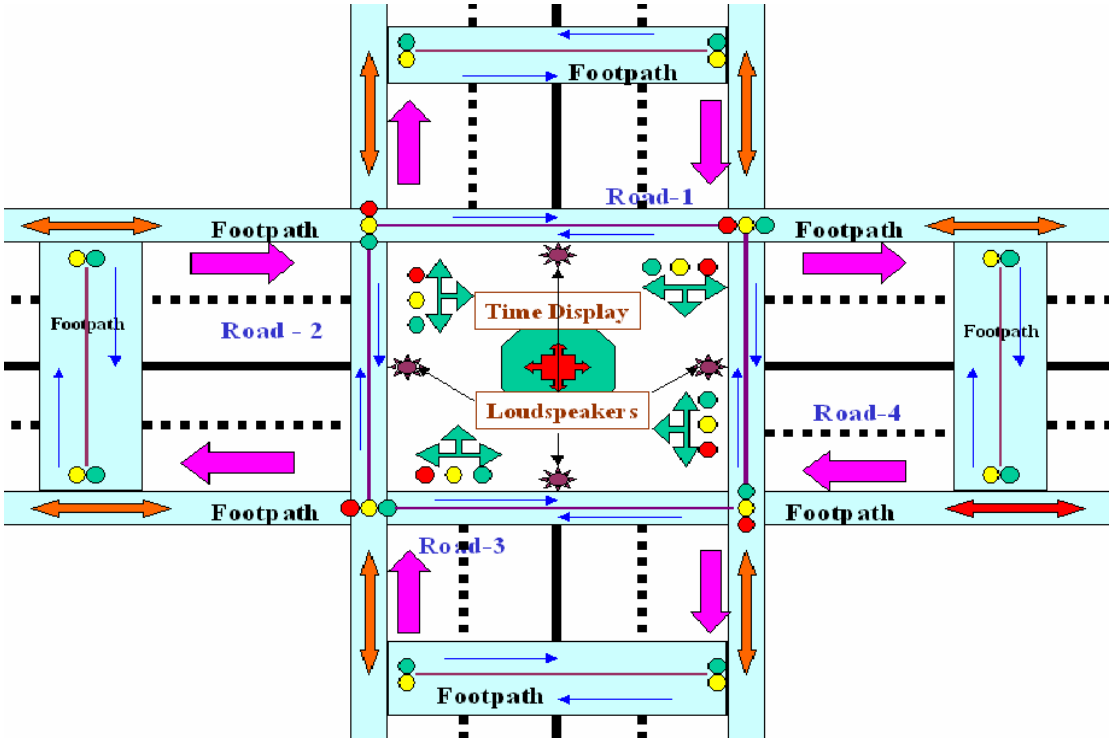

Figure – 1: - Road Junction map

2. ASIC HARDWARE OF THE ASIC SYSTEM

Figure-2 shows the complete hardware diagram of the ASIC device. It consists the following blocks and logic elements.

(1). Mod-Counters: A counter is probably one of the most useful and versatile subsystems in a digital system. A counter driven by a clock can be used to count the number of clock cycles. Since clock pulses occur at known intervals, the counter can be used as an instrument for measuring time and period or frequency [3]. A counter can be synchronous, asynchronous, or a combination of these two types; furthermore, there is the decision of which count to skip. Here for instance, a Mod-5 counter using three flip-flops is to be constructed, which three of the eight discrete states should be skipped. Our purpose here is not to consider all possible counter configurations. Here a Mod-6 counter using three flip-flops is to be constructed, which two of the eight discrete states should be skipped. And a Mod-10 counter using four flip-flops is to be constructed, which two of the six discrete states should be skipped. This circuit gives the perfect timing (seconds and minutes) and state values.

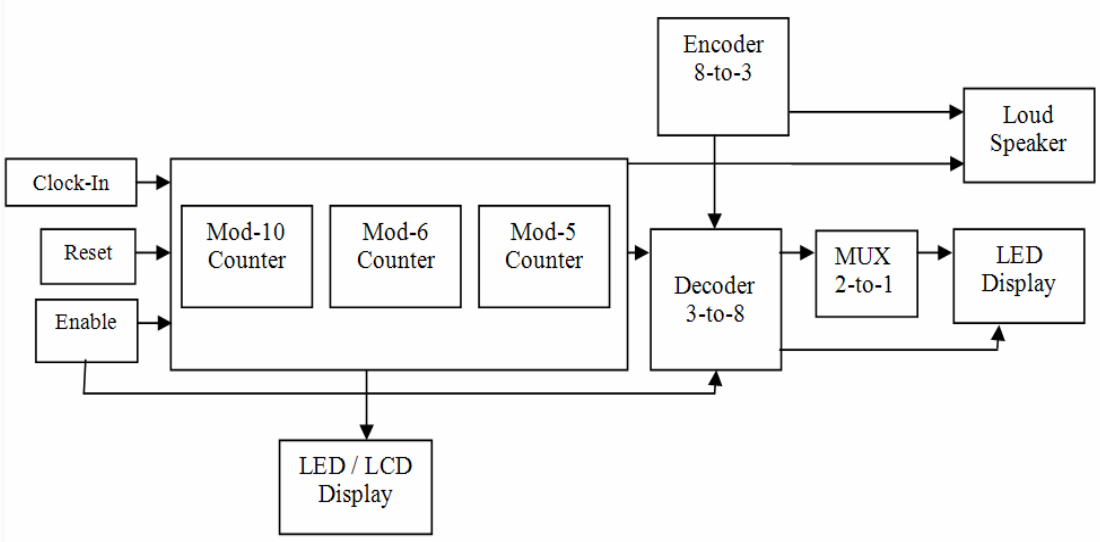

Figure – 2: Basic Hardware of ASIC device

(2). Mid-Decoder: A decoder is similar to a demultiplexer, with one exception – there is no data input. The only inputs are the control bits "ABC". Using the 3-of-8 decoder developed this Mid-Decoder. The logic circuit is called a 3-of-8 decoder because only 1-of- 8 outputs a line is high [4]. For instance, when "ABC" control bits are setting than this Mid-Decoder is skipping the last three logic outputs and considering the only first five-logic values result. This circuit gives the control signals to all the roads and footpaths.

(3). Mid-Encode-Switch: An encoder converts an active input signal into a coded output signal. There are 'n' input lines, only one of which is active. Internal logic within the encoder converts this active input to a coded binary output with 'm' bits [5]. Here we used the 8-of-3-encoder logic circuit, but we have taken only five of the eight switches. Thus we are skipping the remaining three decimal values. That is why it is a Mid-Encode-Switch. This circuit gives the direct state or road operating logic values by pressing desired switch.

(4). Mode-Mux: Multiplex means many into one. A multiplexer is a circuit with many inputs but only one output. By applying control signals, we can steer any input to the output. Thus it is also called a data selector and control inputs are termed select inputs [6]. In this system the 2-to-1 multiplexer used as Mode-Mux to select the mode of operation. Mode-Mux has one input from the first AND3 gate output of Mid-Decoder, second is state-1 or road-1 output logic of the Mid-Encode-Switch and these signals are controlled by the control signal *Enable (logic-1/0)* switch.

(5). Clock Generator: We have had only one clock generator, which is fed to the Mod-10 counter for second's generation. After that it will be divided in to the minutes and state values by using other Mod-Counters.

(6). LEDs: These are indicators of the signals, here we used three colors LEDs i.e., Red for Stop, Green for Go and Yellow for ready. These LEDs are arranged at the corner and facing of the each and every roads and footpaths.

(7). LED/LCD Display: This arrangement is useful to display the timing of the each state. Due to this that we can understand how much time remaining to state change. This timing display is arranged at middle of the junction facing all the roads.

(8). Loudspeaker: This loudspeaker gives sound before changing the signal from present state to next state. This loudspeaker is arranged at the entrance center of the each road.

3. CMOS SIGNAL DECODING CIRTUIT

The Figure-3 shows the CMOS Signal Decoding Circuit, which was developed by using the P-MOS and C-MOS transistors. To develop this we have used the 18 P-MOS and 18 N-MOS transistors. This circuit provides the decoded signals with respect to the timing and control signals to control the different road and color (R/G/Y) signals. This can control the twelve signals which are arranged at four road junction.

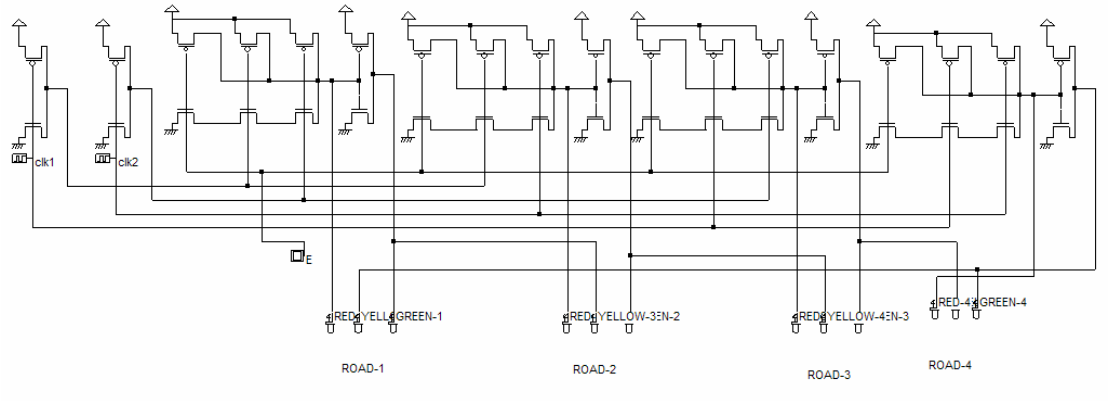

Figure-3: CMOS Signal Decoding Circuit

4. 90nm TECHNOLOGY LAYOUT

We developed the CMOS circuit layout circuit in 90nm technology. Figure-4 shows the 90nm technology layout of CMOS circuit. For this we used power supply 1.2V and 6 metal layers. The DRC was checked and tested all the results. For this the signals, Time low (tl) is 0.475ns, Rise time (tr) is 0.025ns, Time high (th) is 0.475ns and Fall time (tf) is 0.025ns. The clock signal amplitude (A) is 0.30V and Frequency (f) is 1000MHz. This total layout Width is 14.3µm (238 lambda),Height is 4.0µm (67 lambda) and Surf is 57.4µm2 (0.0 mm2).

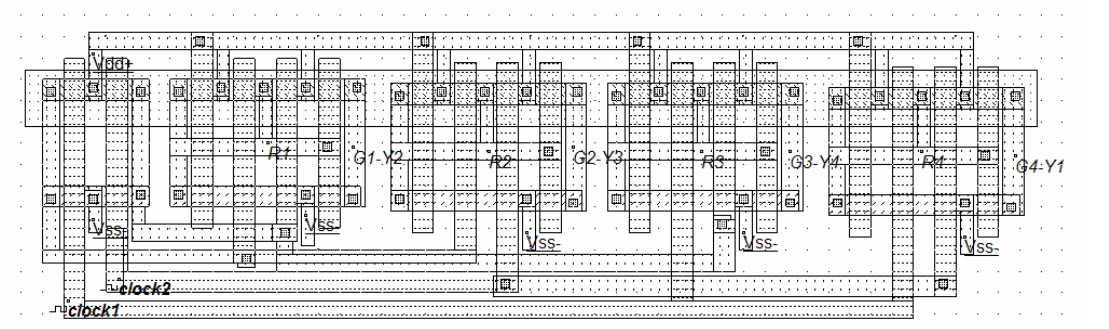

Figure-4: 90nm Technology Layout of ASIC CMOS circuit

5. OPERATION MODES and RESULTS

The ASIC device can be controlled by two modes –

(A). Mode-1 (With Automatic clock)

(B). Mode-2 (With Mid-Encode-Switch)

(A). Mode-1: To select this Mode-1, first we have to *reset* and then *Enable (logic-1)* the system as shown in the flow-chart and state diagram. Now, the device is ready to operate with respect to the clock timing pulse. Time control purpose, we are using Mod-Counters. In this mode by default all roads or states gets red-light signal,

except local footpaths (always gets yellow and green). The time (Maximum: One Minute for each state) display is arranged on the middle of the roads junction. All the roads one after another will get the proper light control signals with respect to the clock timing signals. At the center of main junction signal timings will display on LCD/LED screen. The time is fixed as one minute for Red and Green signals of each road and footpaths. When the state changes time is remaining ten seconds (i.e., after 50 seconds of state start) Yellow light of next state will glow [7]. When the state change time is remaining five seconds (i.e., after 55 seconds of state start) will give sound to indicate state changing. And there are local footpaths, which are useful to cross the same road from one side to another, that, they got always yellow and green signals for look and go type. In this, all the roads and footpaths are two-way type. Once we reset the device this process will be progressed until the power is on. But, only the state-1 must be controlled through the Mode-Mux, which is controlled by the *Enable (logic-1)* and Mid-Decoder. Results are shown in Figure-5.

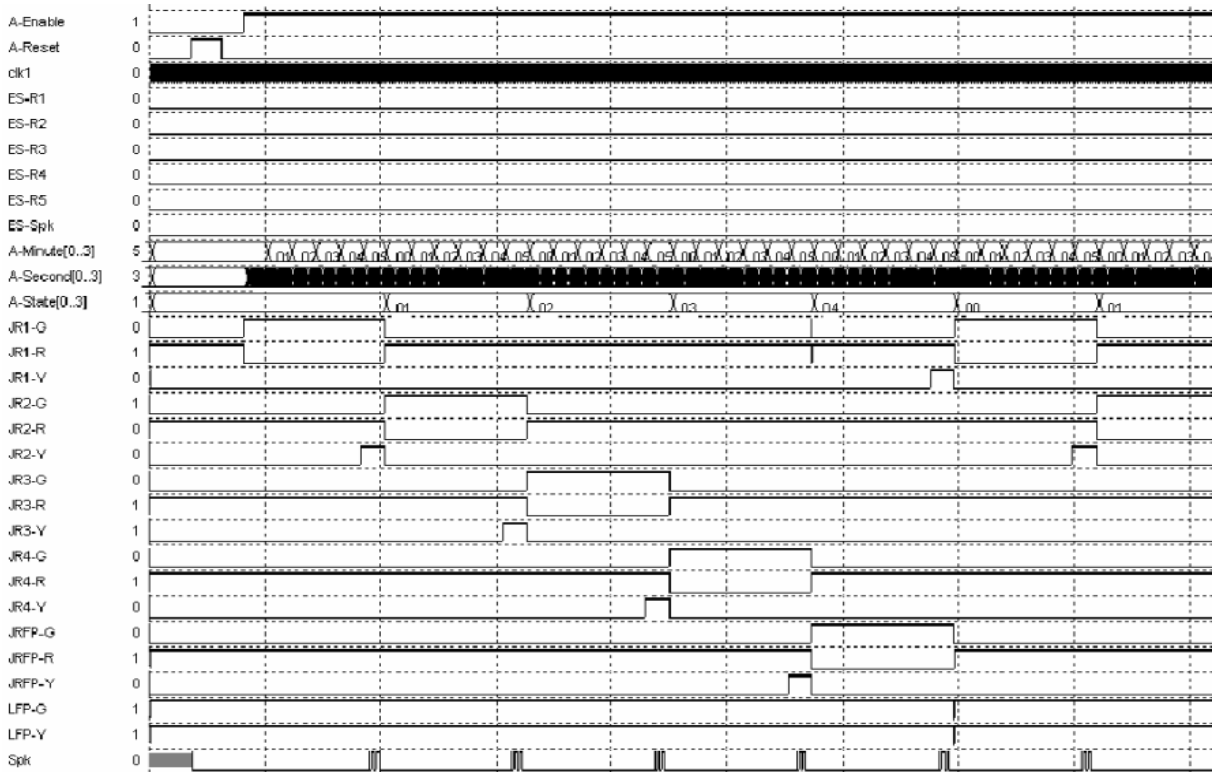

Figure – 5: Mode-1 output waveforms

(B). Mode-2: This Mode-2 operation is quite different from the previous one but the main difference is that it can operate with out limited timing and proper state sequence rotation. How to operate this mode is shown in the flow-chart and state diagram. In this mode by default all roads or states gets red-light signal, except local footpaths (always gets yellow and green) [8]. But the state-1 must control through the Mode-Mux, which is controlled by the *Enable (logic-0)* and Mid-Encode-Switch. In this mode, there is no use of yellow lights only the loudspeaker sound blows before the state changing. After the loudspeaker sound, must have to give red signal to all the roads or states. I.e., we must press the loudspeaker key before going to press the next state key. In this there is no limited time for each state and proper sequence. This mode is useful when traffic is heavy at particular roads, needed to control directly with desired timing and sequence of state. Results are shown in Figure-6.

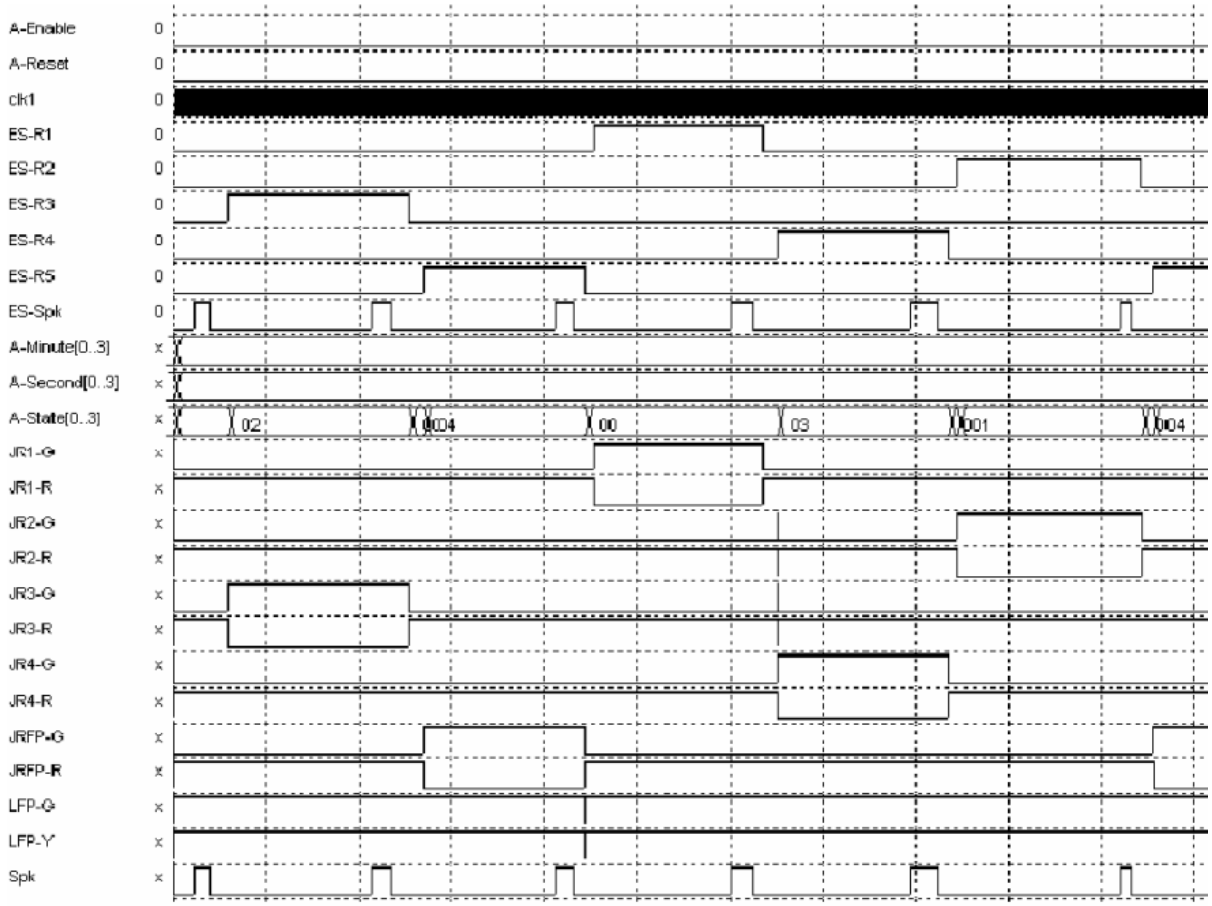

Figure – 6: Mode-2 output waveforms

6. CONCLUSION

A simple optimized, low voltage and cost effective ASIC device for traffic light control has been designed, fabricated and tested successfully for its functionality. This compact design permits the user to select any type of control functional modes, i.e., by automatic clock generator to control the traffic of roads automatically and Mid-Encode-Switch circuits to control traffic of desired roads of the junction directly. The CMOS circuit and 90nm Layout is developed and tested its functionality.

7. REFERENCES

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